

# Overlay Strategy in EUV Lithography Era

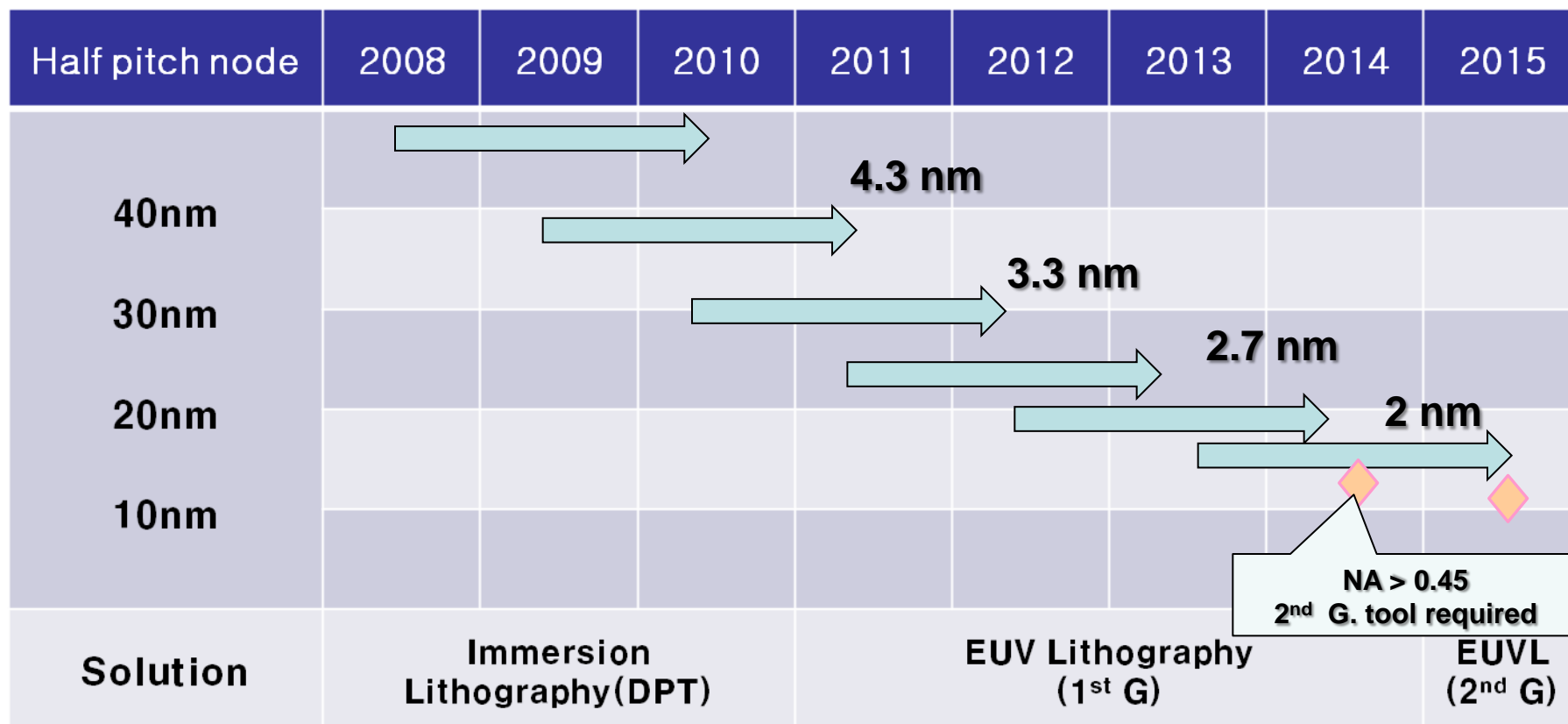
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- **Device overlay spec. roadmap**
- **EUV overlay budget analysis**
- **EUV ADT vs. Immersion MMO basic performance**
- **EUV overlay impact breakdown**
- **In\_field distortion analysis**
- **Summary**

# Device Overlay Spec\*. Roadmap



\*Machine budget only

- ◆ Overlay spec. DRAM device critical layer
- ◆ Trend continued with Device scaling down trend

# Solutions for 2X Node DRAM

		EUVL	DPT	NIL
Imaging	Dense L/S	OK	OK	OK
	Random L/S	OK	Difficult	OK
	Dense C/T	OK	Very difficult	OK
	Small C/T	OK	Difficult	OK
Overlay		~7nm	~5nm	~ 20nm
Cost ( comparing ArFi)		2X	Dense L/S : 2X Random : ~3X Dense C/T : 4X	? ( > 2X)
Timing		2010: PPT 2012: HVM	Ready	Not Ready

# New Comer in 'Factory'

- ◆ **Scanner**
  - Need special care about contamination
- ◆ **Reticle**
  - Need additional OPC step
  - Need new pods (No Pellicle)
  - Need stricter rules to prevent defects
- ◆ **Resist**
  - Need specific outgassing spec.
  - May need additional process
- ◆ **CD metrology**
  - Need advanced metrology tools
- ◆ **Overlay strategy**
  - ??

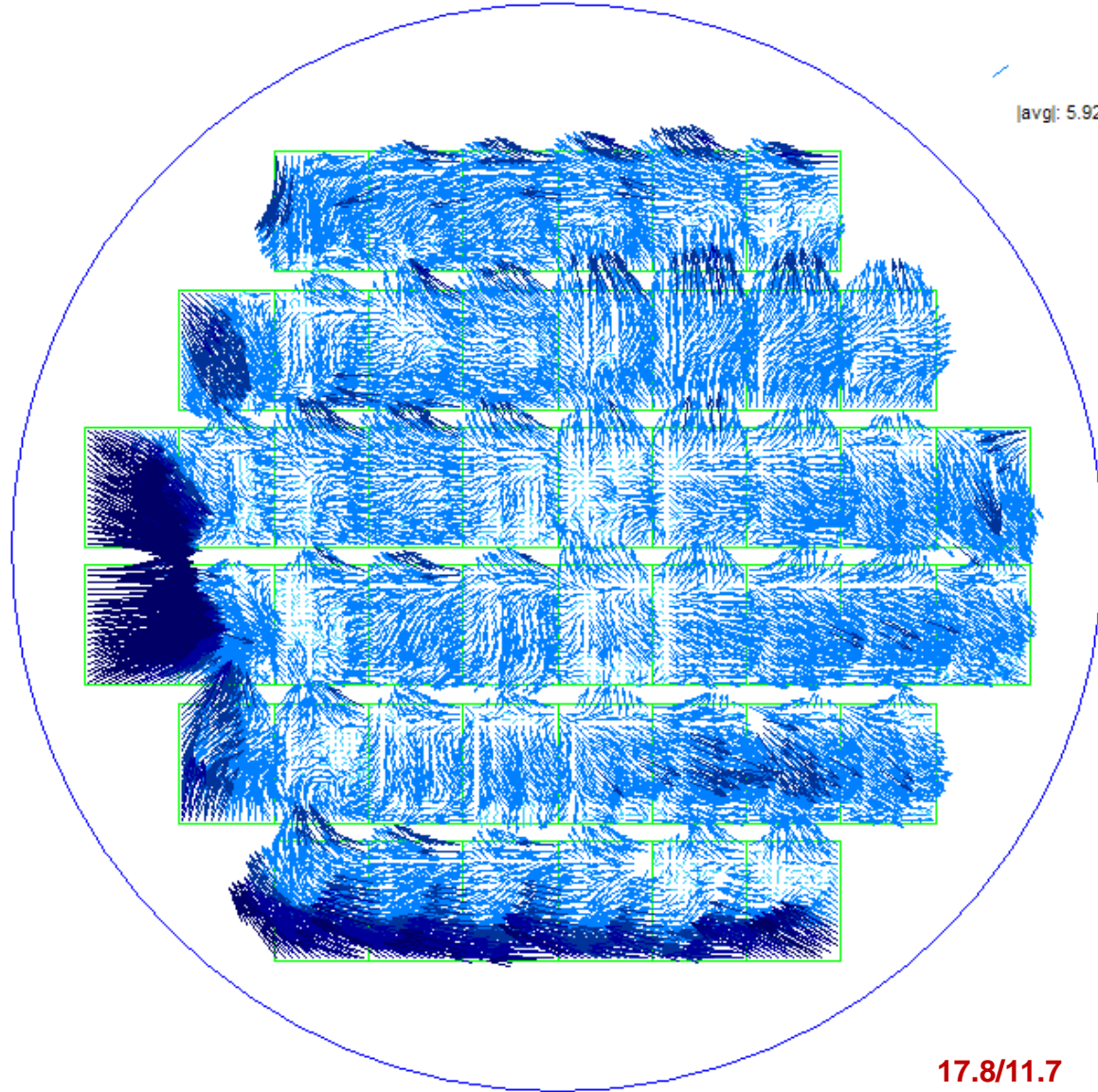
# EUV Overlay Budget -What is new?

Budget item	Issue	Budget involved
Reticle shape imperfection	<ul style="list-style-type: none"><li>• Reticle figure impacts on overlay because of non-telecentricity</li></ul>	<5 nm
Reticle electro static clamp	<ul style="list-style-type: none"><li>• Lack of knowledge about clamping distortion</li></ul>	<4 nm
Stiff mirror block	<ul style="list-style-type: none"><li>• Limited correction potential</li></ul>	< 3 nm
Wafer electro static clamp	<ul style="list-style-type: none"><li>• Wafer vs. ESC interaction</li></ul>	<2 nm
System heating	<ul style="list-style-type: none"><li>• Stage/mirror heating by IR</li></ul>	Budget unknown



# ADT vs. Immersion MMO - Current Status

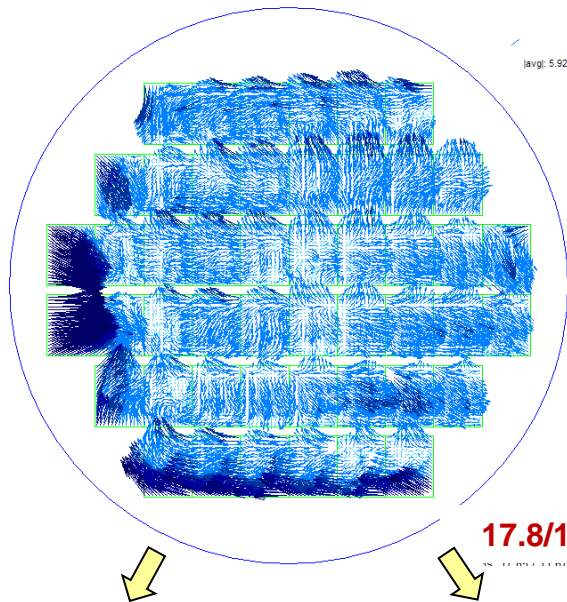
SAMCO 100th Anniversary: Everyone's invited™



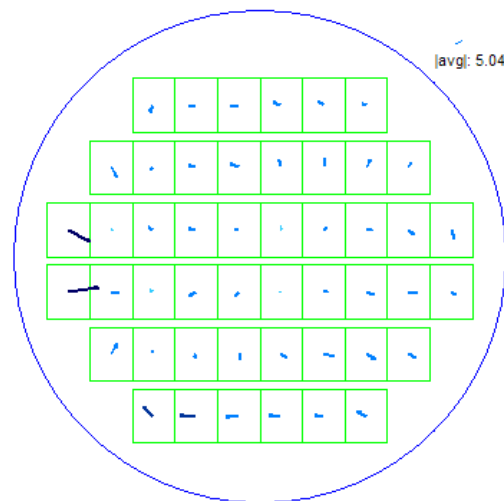
17.8/11.7

# ADT vs. Immersion MMO - Current Status

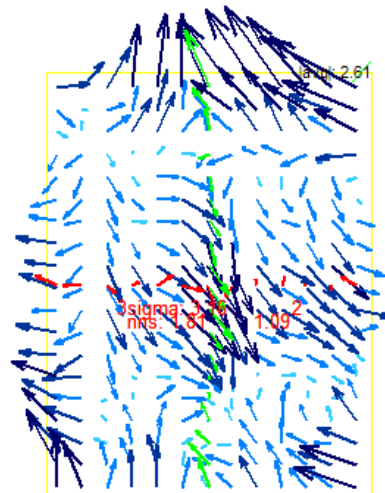
everyone's invited™



17.8/11.7



15.7/9



5.9/6.2

Total overlay error ~ 18 nm

Wafer grid error ~ 16 nm

Shot distortion ~ 6 nm

## Symptoms

- Wafer stage indexing distortion
- Wafer table local distortion
- Reticle distortion
- Illumination distortion
- Scanning distortion



# Wafer Grid Distortion - Trend

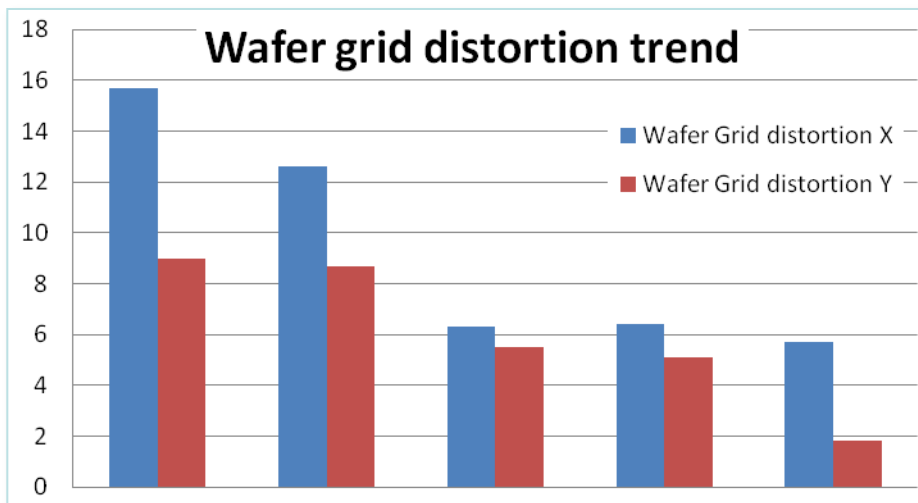
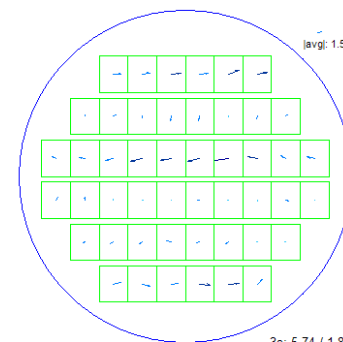
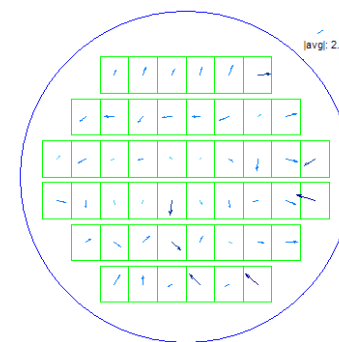
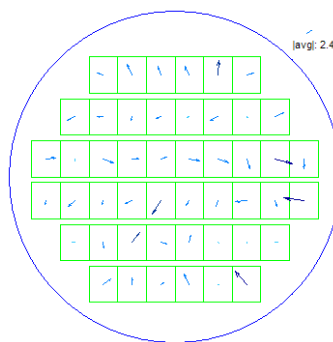
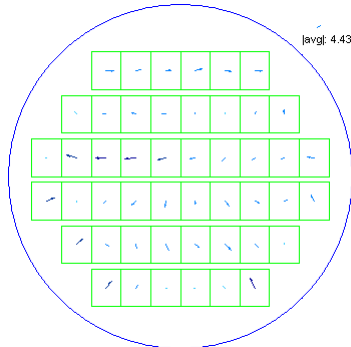
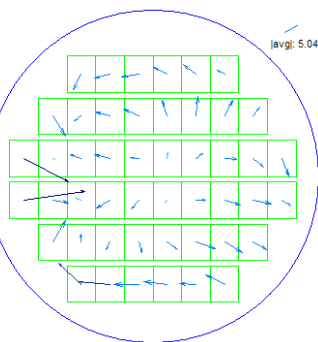
Test 1

Test 2

Test 3

Test 4

Test 5



## Expected grid matching performance

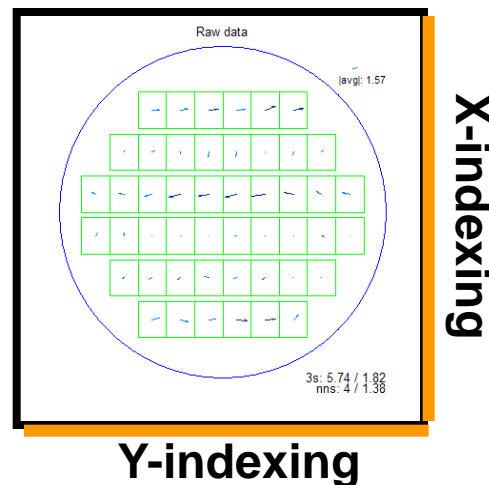
- X: 16 nm  $\rightarrow$  6 nm
- Y: 7 nm  $\rightarrow$  2 nm

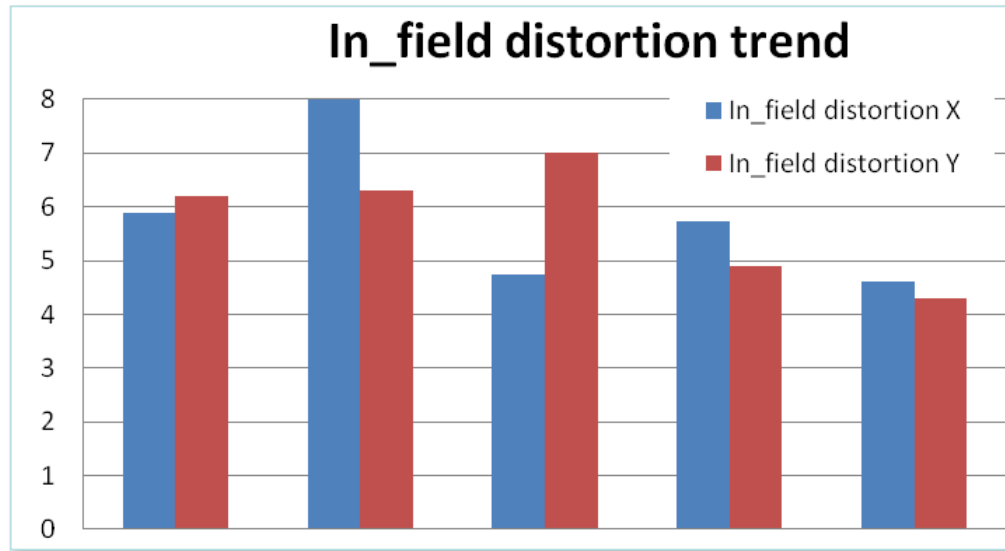
## Distortion drift observed

- X-direction

# Wafer Grid Distortion - Interpretation

- ◆ Y indexing is stable and can be tamed
  - Range: ~ 1.2 nm
- ◆ X indexing shows large drift
  - Seems faulty hardware
  - 2 nm - 4 nm
- ◆ Expect <2 nm performance
  - if good wafer clamping quality is secured

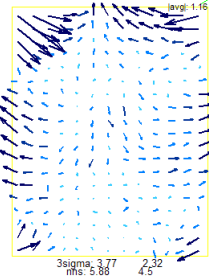




- ◆ **In\_field distortion fingerprint**
  - Budget: ~5 – 6 nm
  - Have Similar shape
  - Localized distortion
  - Localized deviation from fingerprint

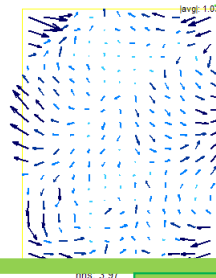
# Clamping Distortion - Breakdown

Test 1

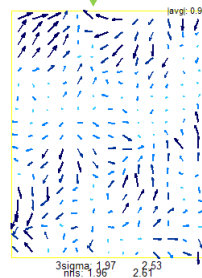


Group 1

Test 3

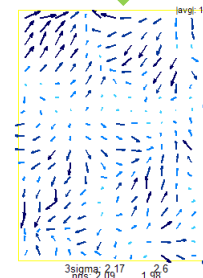


Test 2

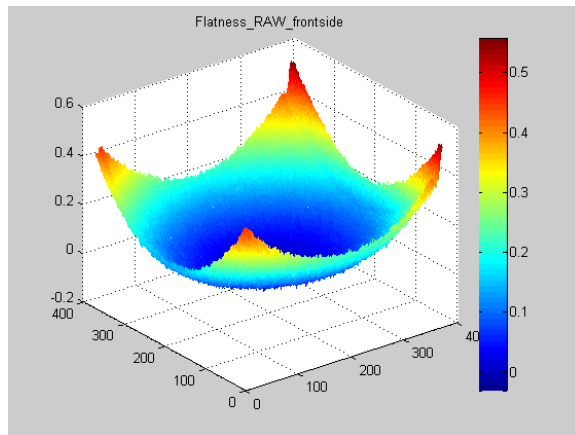
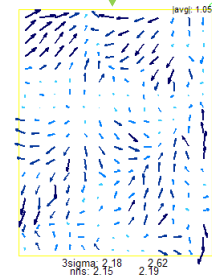


Group 2

Test 4



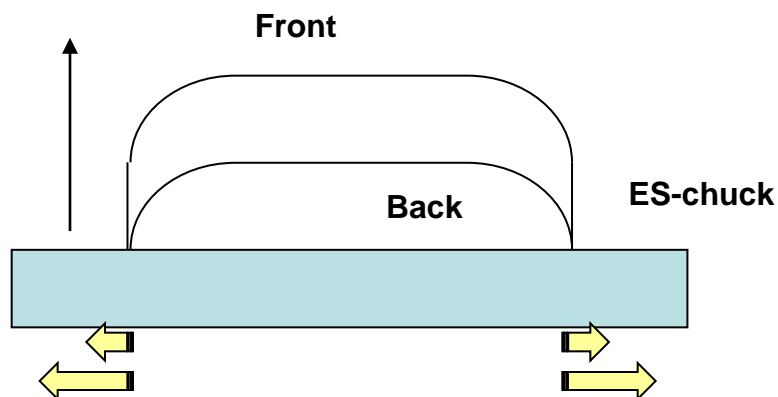
Test 5



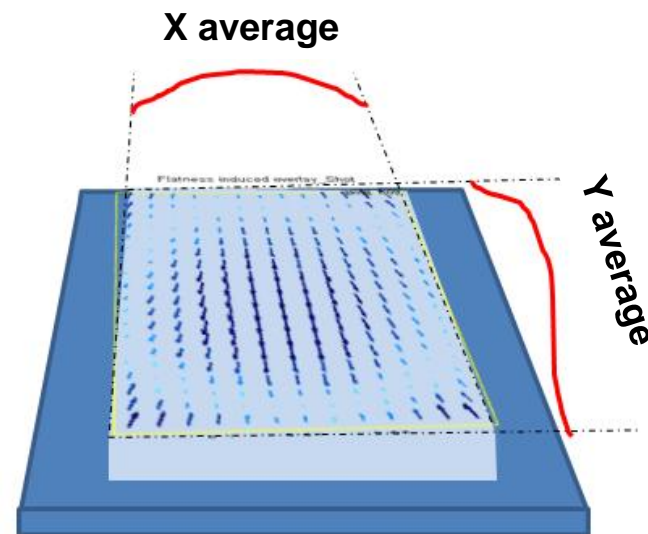
Backside of the Reticle  
Bow after process

- ◆ Current reticle has 600 – 800 nm backside bow
- ◆ Reticle Bow assumes to induce Clamping distortion and variation
  - Not in similar ways

# Reticle impact on In-field fingerprint



Chucking distortion/variation



Reticle figure impact on budget breakdown

- ◆ Reticle shape and figure (bow and flatness) both impact on fingerprint
- ◆ 'HOLY' reticle required to avoid reticle shape impact



- ◆ **EUV scanner setup**
  - Cannot execute proper setup
- ◆ **Scanner drift during usage**
  - Mode change
  - Scanner NCE + Reticle NCE
- ◆ **EUV Single Machine Overlay**
  - Reticle 2 Reticle matching required
  - Reticle dedication required
- ◆ **EUV Mix and Match with Immersion**
  - System fingerprint matching not possible
  - Reticle 2 Reticle matching required
  - Reticle dedication required

# Solution Needed

## Scanner Manufacturer

- Minimize clamping distortion

## Blank Manufacturer

- Improved Sub/Blank
- Measurement accuracy

- Holy reticle
- Understood spec.
- Eval. results

## Device Manufacturer

- Field adaptation

## ◆ EUV overlay – Wafer term

- Wafer grid distortion can be addressed with a conventional way once the wafer electro-static clamping repro confirmed.
- Wafer electro-static clamping must be localized distortion free.

## ◆ EUV overlay – In\_field term

- In\_field distortion cannot be broken down because of cross-talk among
  - Reticle fingerprint (by shape and figure)
  - Aberration distortion
  - Scanning distortion
- Clamping distortion/variation from Reticle bow
  - Minimize bow and clamping impact

## ◆ ‘HOLY’ reticle is required to confirm the scanner related in\_field distortion.

- 30 nm flatness P-V spec.
- Not defect free

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